ABSTRACT

A rectangular parallelepiped projecting portion (21) having a height of H_B and a width of W_B is formed on a silicon substrate, and a gate oxide film is formed on a part of the top surface and the side surface of the projecting portion (21), thereby generating a MOS transistor. By connecting in parallel a p-channel MOS transistor and an n-channel MOS transistor produced as described above, a switch of a switched capacitor circuit is configured, thereby reducing a leak current and a DC offset of the switched capacitor circuit.